REMARKS

Claims 1-8 are pending in this application. Claims 1-3, 5 and 8 are rejected; and claims 4, 6 and 7 are objected to in this application. Keeping in mind the Examiner's recommendation to rewrite claims 4, 6 and 7 in independent form, claims 4, 6 and 7 are amended hereby.

Responsive to the rejection of claims 1 and 8 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,212,434 (Hsieh) Applicants respectfully traverse the rejection.

Hsieh discloses a phase-locked step motor speed servo controller, including motor 50, speed detector 60 and phase detector 10. Phase detector 10 having a first input port V and a second input port R. First input port V is connected to the output of speed detector 60 to receive feedback signal $P_1(t)$ having phase θ_1 and second input port R is connected to reference signal $P_2(t)$ whose frequency is f_2 and phase is θ_2. The difference between the phase θ_1 of feedback signal $P_1(t)$ and phase θ_2 of reference signal $P_2(t)$ is the phase error θ_e ($\theta_e = \theta_1 - \theta_2$). Phase error θ_e will cause up-down counter 22 to increase or decrease proportional to $\theta_e / 2\pi$, the count of which is utilized to alter output voltage V_o, which is proportional to θ_e as shown in Fig. 5. V_o increases if θ_e indicates a phase lag, causing an increase in the rate of pulses sent to motor 50 in order to increase the speed of motor 50. Conversely, V_o decreases if θ_e indicates a phase lead, causing a decrease in the rate of pulses sent to motor 50 in order to decrease the speed of motor 50.

In contrast, claim 1 recites in part:

> generating a plurality of digital signals defining <u>a reference pulse train with a frequency dependent upon said reference signal</u>;
>
> providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining <u>a feedback pulse train having a frequency</u>;
>
> <u>comparing said frequency of said reference pulse train with said frequency of said feedback pulse train</u>.

(Emphasis added) Applicants submit that such structure is neither taught, disclosed nor suggested by Hsieh or any of the other cited references, alone or in combination, and includes distinct advantages thereover.

Hsieh teaches the use of the comparison of the phase of a signal generated by a speed detector to the phase of a reference signal to adjust the input to a motor. However, Hsieh fails to disclose or suggest the generating of a reference pulse train, which is not dependent on the phase of the reference signal, and using the reference pulse train and the feedback pulse train to generate control signals for the correction of the speed of a motor. Accordingly, Applicants submit that claim 1, and claim 8 depending therefrom, are now in condition for allowance, which is hereby respectfully requested.

Claims 2, 3 and 5 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,212,434 (Hsieh) in view of either U.S. Patent No. 4,494,509 (Long) or U.S. Patent No. 6,043,695 (O'Sullivan). However, claims 2, 3 and 5 depend from claim 1 which has been placed in condition for allowance for the reasons given above. Accordingly, Applicants submit that claims 2, 3 and 5 are now in condition for allowance, which is hereby respectfully requested.

For the foregoing reasons, Applicants submit that no combination of the cited references teaches, discloses or suggests the subject matter of the claims as amended. The pending claims are therefore in condition for allowance, and Applicants respectfully request withdrawal of all rejections and allowance of the claims.

In the event Applicants have overlooked the need for an extension of time, an additional extension of time, payment of fee, or additional payment of fee, Applicants hereby conditionally petition therefor and authorize that any charges be made to Deposit Account No. 20-0095,

Should any question concerning any of the foregoing arise, the Examiner is invited to telephone the undersigned at (219) 897-3400.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on: May 14, 2001.

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Signature

May 14, 2001
Date

ATTACHMENT A: MARKED-UP COPY SHOWING AMENDMENTS

IN THE CLAIMS

4. (Amended) [The method of regulating a target system of claim 3, wherein said step of generating said control signal comprises the further substeps of:]

<u>A method of regulating a target system, comprising the steps of:</u>

<u>providing a reference signal;</u>

<u>generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;</u>

<u>providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;</u>

<u>comparing said frequency of said reference pulse train with said frequency of said feedback pulse train;</u>

<u>substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train;</u>

<u>generating a control signal dependent upon said comparison, said generating step including the substeps of:</u>

<u>generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train;</u>

counting up from zero with a first proportional clock CP1 at a frequency fP1 when said digital signals of said proportional error pulse train are in a high state;

resetting said first proportional clock CP1 to zero when said digital signals of said proportional error pulse train are in a low state;

loading a current value of said first proportional clock CP1 into a second proportional clock CP2 each time said first proportional clock CP1 transitions from a high state to a low state;

counting down from said loaded current value with said second proportional clock CP2 at a frequency fP2 until a zero value is reached; and

determining a proportional error term representing a time average of a signal which is held high while said second proportional clock CP2 is in a high state and held low while said second proportional clock CP2 is in a zero state, said control signal being dependent upon said proportional error term; and

providing said control signal as an input to said target system.

6. (Amended) [The method of regulating a target system of claim 5, wherein said step of generating said control signal comprises the further substeps of:]

A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train, and substantially aligning a leading edge of each digital signal in said reference pulse train

with a leading edge of each digital signal in said feedback pulse train;

generating a control signal dependent upon said comparison, said generating step including the substeps of:

generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train;

generating an error direction pulse train including a plurality of digital signals, each said digital signal representing a directionality of said error between said corresponding pair of aligned digital signals;

counting up from zero with a first integral clock CI1 at a frequency fI1 when said digital signals of said proportional error pulse train are in a high state and said digital signals of said error direction pulse train are simultaneously in a high state;

counting down with said first integral clock CI1 at said frequency fI1 when said digital signals of said proportional error pulse train are in a high state and said digital signals of said error direction pulse train are in a low state;

maintaining said first integral clock CI1 at a current value when said digital signals of said proportional error pulse train are in a low state;

loading a current value of said first integral clock CI1 into a second integral clock CI2 each time said first integral clock CI1 transitions from a high state to a low state;

counting down from said loaded current value with said second integral clock CI2 at a frequency fI2 until a zero value is reached; and

determining an integral error term representing a time average of a signal which is held high while said second integral clock CI2 is in a high state and held low while said second integral clock CI2 is in a zero state, said control signal being dependent upon said integral error term; and

providing said control signal as an input to said target system.

7. (Amended) [The method of regulating a target system of claim 3, wherein said step of generating said control signal comprises the further substeps of:]

A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train, and substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train;

generating a control signal dependent upon said comparison, said generating step including the substeps of:

generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train;

counting up from zero with a first derivative clock CD1 at a frequency fD1

when said digital signals of said proportional error pulse train are in a high state;

subtracting a current state of said first derivative clock CD1 from a current state of a register R each time said first derivative clock CD1 transitions from a high state to a low state;

loading said subtracted state into a second derivative clock CD2;

loading said current state of said first derivative clock CD1 into said register R;

resetting said first derivative clock CD1 to zero;

counting down with said second derivative clock CD2 at a frequency fD2 after said subtracted state is loaded therein;

maintaining said first integral clock CI1 at a current value when said digital signals of said proportional error pulse train are in a low state; and

determining a derivative error term representing a time average of a signal which is held high while said second derivative clock CD2 is in a high state and held low while said second derivative clock CD2 is in a zero state, said control signal being dependent upon said derivative error term; and

providing said control signal as an input to said target system.